



TFT LCD Preliminary Specification

MODEL NO.: V520H1 - L05

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**REVISION HISTORY**

Version	Date	Page	Section	Description
Ver.1.0	Apr.10, 2007	All	All	Preliminary Specification was first issued.

1. GENERAL DESCRIPTION

1.1 OVERVIEW

V520H1-L05 is a 52" TFT Liquid Crystal Display module with 28-CCFL Backlight unit and 2ch-LVDS interface. This module supports 1920 x 1080 HDTV format and can display true 16.7M colors (8-bit/color).

The inverter module for backlight is built-in.

1.2 FEATURES

- High brightness (550 nits)
- High contrast ratio (1500:1)
- Fast response time (Gray to gray average 6.5 ms)
- High color saturation (NTSC 92%)
- Full HDTV (1920 x 1080 pixels) resolution, true HDTV format
- DE (Data Enable) only mode
- LVDS (Low Voltage Differential Signaling) interface
- Optimized response time for 50/60 Hz frame rate
- Ultra wide viewing angle : Super MVA technology
- 180 degree rotation display option
- RoHS compliance

1.3 APPLICATION

- Standard Living Room TVs.
- Public Display Application.
- Home Theater Application.
- MFM Application.

1.4 GENERAL SPECIFICATIONS

Item	Specification	Unit	Note
Active Area	1152 x 648 (52.037")	mm	(1)
Bezel Opening Area	1166.0x662.0	mm	
Driver Element	a-si TFT active matrix	-	-
Pixel Number	1920x R.G.B. x 1080	pixel	-
Pixel Pitch(Sub Pixel)	0.2 (H) x 0.2 (V)	mm	-
Pixel Arrangement	RGB vertical stripe	-	-
Display Colors	16.7M	color	-
Display Operation Mode	Transmissive mode / Normally black	-	-
Surface Treatment	Hard coating 3H Low reflection coating< 1.3% reflection	-	(2)

Note (1) Please refer to the attached drawings in chapter 9 for more information about the front and back outlines.

Note (2) The spec of the surface treatment is temporarily for this phase. CMO reserves the rights to change this feature.

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Issue Date: Apr.10.2007

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Preliminary**1.5 MECHANICAL SPECIFICATIONS**

Item			Min.	Typ.	Max.	Unit	Note
Module Size	Horizontal (H)		1224.5	1226	1227.5	mm	(1), (2)
	Vertical (V)		718.0	719.2	720.4	mm	
	Depth (D)	To inv cover	56.0	57.5	59.0	mm	
		To rear plate	38.5	40	41.5	mm	
Weight				19600		g	-

Note (1) Please refer to the attached drawings for more information of front and back outline dimensions.

Note (2) Module Depth does not include connectors.

2. ABSOLUTE MAXIMUM RATINGS

2.1 ABSOLUTE RATINGS OF ENVIRONMENT

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Storage Temperature	T _{ST}	-20	+60	°C	(1)
Operating Ambient Temperature	T _{OP}	0	50	°C	(1), (2)
Shock (Non-Operating)	S _{NOP}	- ±X, ±Y ±Z	40	G	(3), (5)
			30		
Vibration (Non-Operating)	V _{NOP}	-	1.0	G	(4), (5)

Note (1) Temperature and relative humidity range is shown in the figure below.

(a) 90 %RH Max. ($T_a \leq 40\text{ }^{\circ}\text{C}$).

(b) Wet-bulb temperature should be 39 °C Max. ($T_a > 40\text{ }^{\circ}\text{C}$).

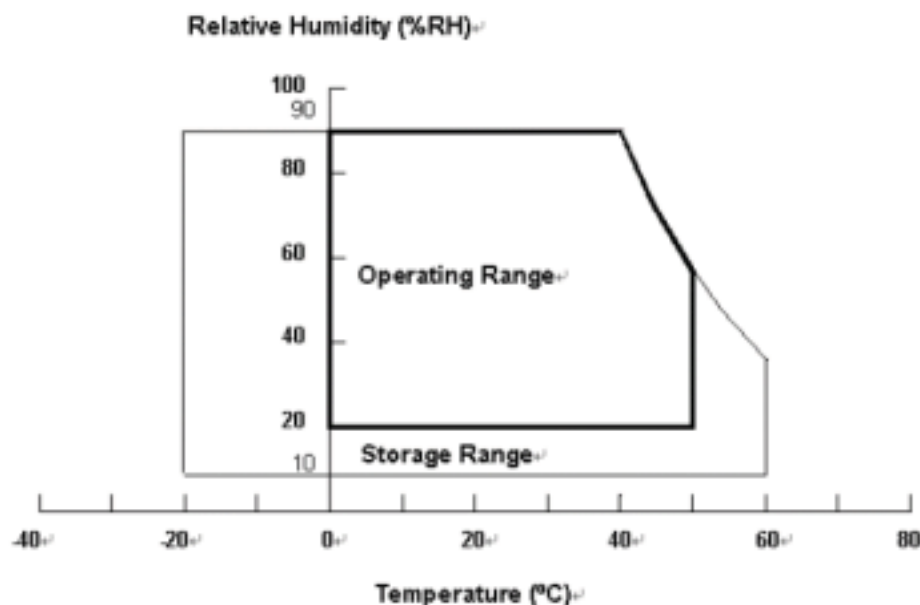
(c) No condensation.

Note (2) The maximum operating temperature is based on the test condition that the surface temperature of display area is less than or equal to 65 °C with LCD module alone in a temperature controlled chamber. Thermal management should be considered in final product design to prevent the surface temperature of display area from being over 65 °C. The range of operating temperature may degrade in case of improper thermal management in final product design.

Note (3) 11 ms, half sine wave, 1 time for $\pm X$, $\pm Y$, $\pm Z$.

Note (4) 10 ~ 200 Hz, 10 min, 1 time each X, Y, Z.

Note (5) At testing Vibration and Shock, the fixture in holding the module has to be hard and rigid enough so that the module would not be twisted or bent by the fixture.



2.2 Package storage

When storing modules as spares for a long time, the following precaution is necessary.

- (a) Do not leave the module in high temperature, and high humidity for a long time. It is highly recommended to store the module with temperature from 0 to 35°C at normal humidity without condensation.
- (b) The module shall be stored in dark place. Do not store the TFT-LCD module in direct sunlight or fluorescent light.

2.3 ELECTRICAL ABSOLUTE RATINGS

2.3.1 TFT LCD MODULE

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Power Supply Voltage	V_{CC}	-0.3	13.5	V	(1)
Logic Input Voltage	V_{IN}	-0.3	3.6	V	

2.3.2 BACKLIGHT INVERTER UNIT

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Lamp Voltage	V_W	—	3000	V_{RMS}	

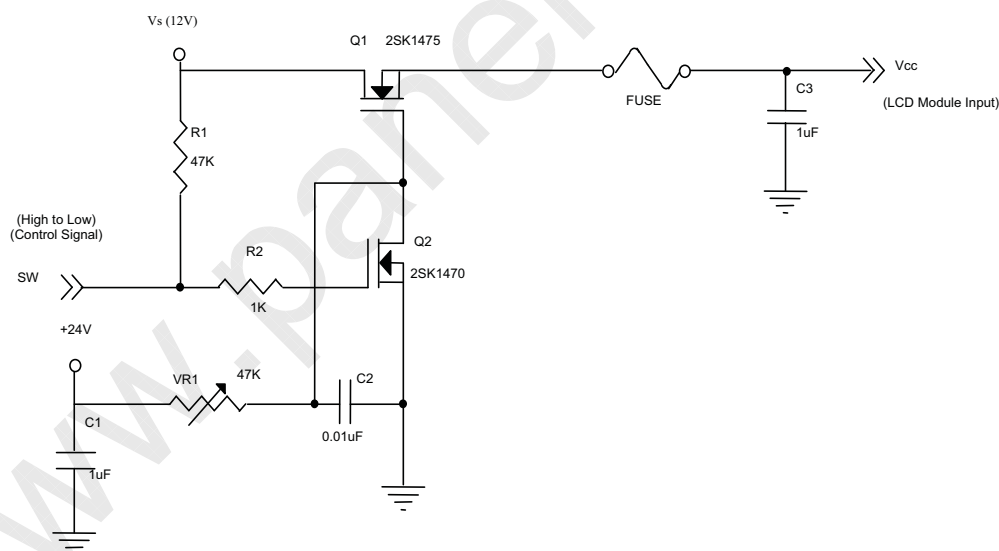
3. ELECTRICAL CHARACTERISTICS

3.1 TFT LCD MODULE (Ta = 25 ± 2 °C)

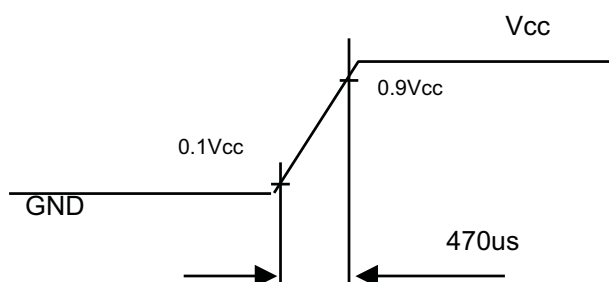
Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Power Supply Voltage		V _{CC}	10.8	12	13.2	V	(1)
Power Supply Ripple Voltage		V _{RP}	-	-	350	mV	
Rush Current		I _{RUSH}	-	-	4.5	A	(2)
Power Supply Current	White	I _{CC}	-	1.5	2.1	A	(3)
	Black		-	0.6	-	A	
	Vertical Stripe		-	1.1	-	A	
LVDS Interface	Differential Input High Threshold Voltage	V _{LVTH}	-	-	100	mV	
	Differential Input Low Threshold Voltage	V _{LVTL}	-100	-	-	mV	
	Common Input Voltage	V _{LVC}	1.125	1.25	1.375	V	
	Terminating Resistor	R _T	-	100	-	ohm	
CMOS interface	Input High Threshold Voltage	V _{IH}	2.7	-	3.3	V	
	Input Low Threshold Voltage	V _{IL}	0	-	0.7	V	

Note (1) The module should be always operated within the above ranges.

Note (2) Measurement condition:



Vcc rising time is 470us





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Preliminary

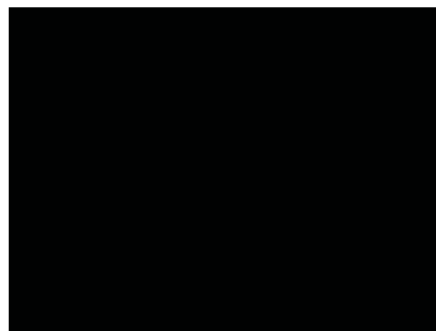
Note (3) The specified power supply current is under the conditions at $V_{cc} = 12\text{ V}$, $T_a = 25 \pm 2\text{ }^{\circ}\text{C}$, $f_v = 60\text{ Hz}$, whereas a power dissipation check pattern below is displayed.

a. White Pattern



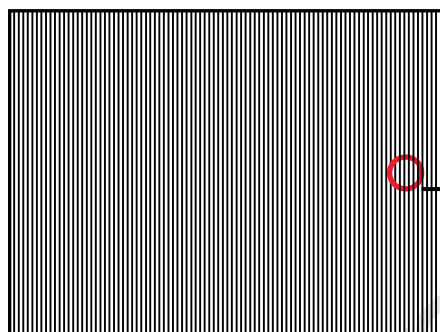
Active Area

b. Black Pattern

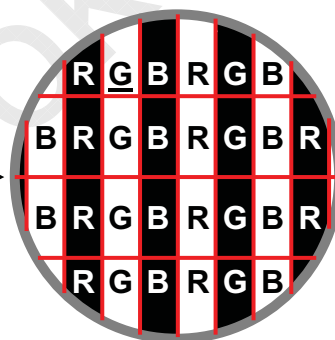


Active Area

c. Vertical Stripe Pattern



Active Area



3.2 BACKLIGHT UNIT

3.2.1 CCFL (Cold Cathode Fluorescent Lamp) CHARACTERISTICS ($T_a = 25 \pm 2^\circ\text{C}$)

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Lamp Input Voltage	V_L	-	1600	-	V_{RMS}	-
Lamp Current	I_L	5.5	6.0	6.5	mA_{RMS}	(1)
Lamp Turn On Voltage	V_S	-	-	2640	V_{RMS}	$T_a = 0^\circ\text{C}$
		-	-	2440	V_{RMS}	$T_a = 25^\circ\text{C}$
Operating Frequency	F_L	40	-	70	KHz	
Lamp Life Time	L_{BL}	50,000	60,000	-	Hrs	(2)

3.2.2 INVERTER CHARACTERISTICS ($T_a = 25 \pm 2^\circ\text{C}$)

3.2.2.1 BALANCE BOARD CONFIGURATION

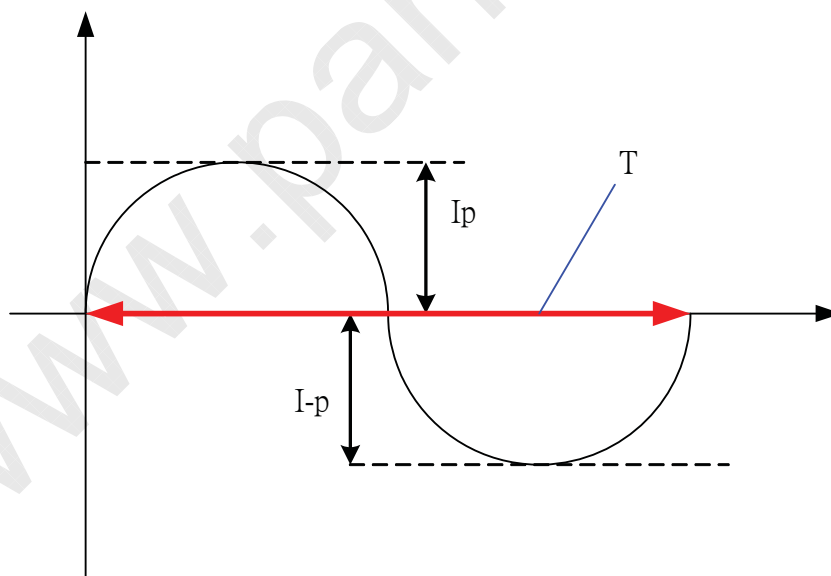


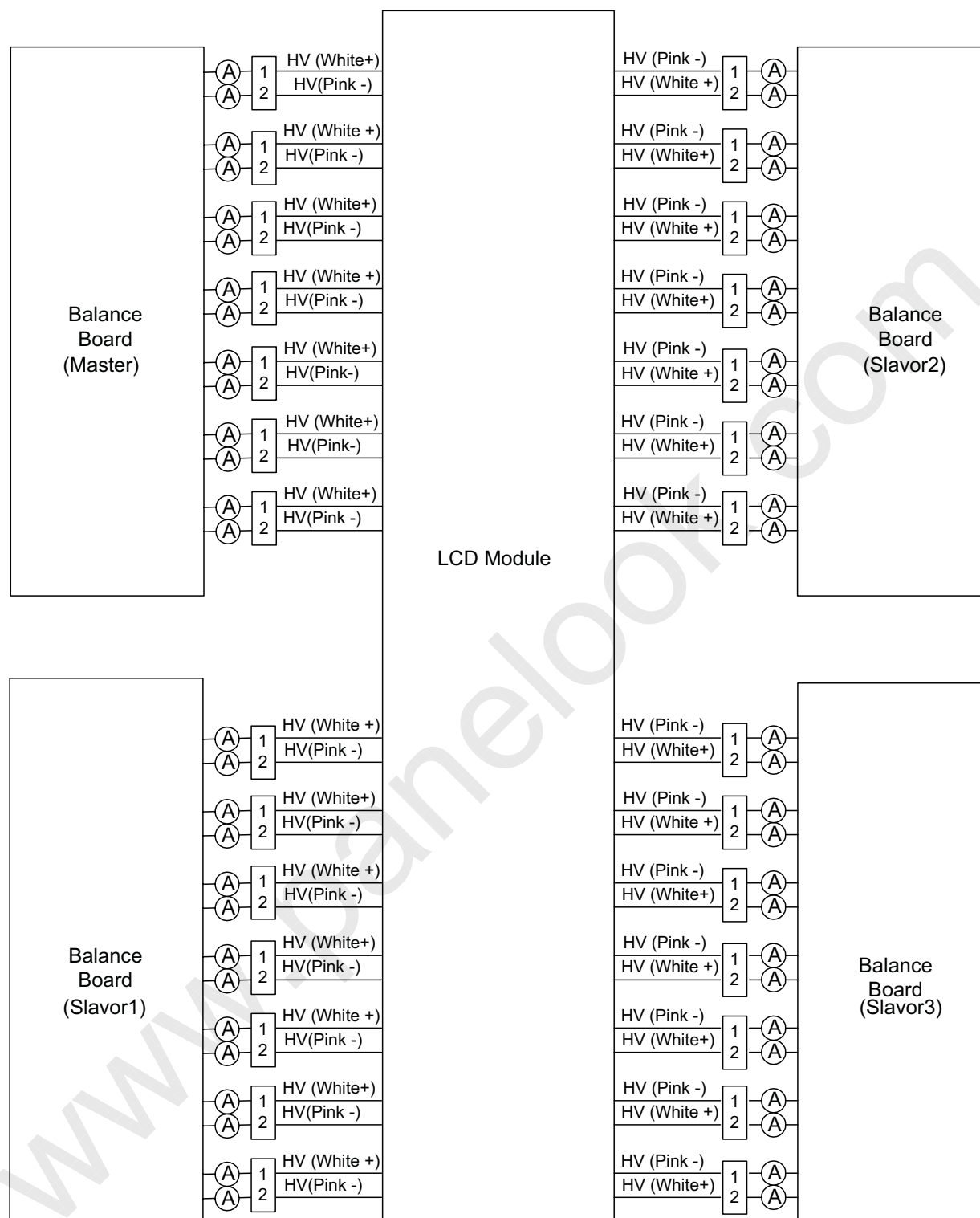
3.2.2.1 BALANCE BOARD SPECIFICATION

Parameter		Symbol	Value			Unit	Note	
			Min.	Typ.	Max.			
Input High Voltage		V_{HV}	1600	1720	1840	V	(1)	Lamp Voltage
Total Input Current of Each HV		Lin(HV)	157.5	175	192.5	mA	(2)	
Operating Frequency		Fop	47	50	53			Switching Frequency
Lamp Current		Iout	5.8	6.0	6.2	mA		
Lamp Detect	High (Normal)	LD	-	12	13.5	V		
	Low (LD)		0	-	0.8	V		
Dimming Frequency		F_{DIM}	150	160	170	Hz		
Dimming Duty-Ratio		D_{PWM}	20	-	100	%		Bright Control

Note (1) Lamp current is measured by utilizing AC current probe and its value is average by measuring master and slave board.

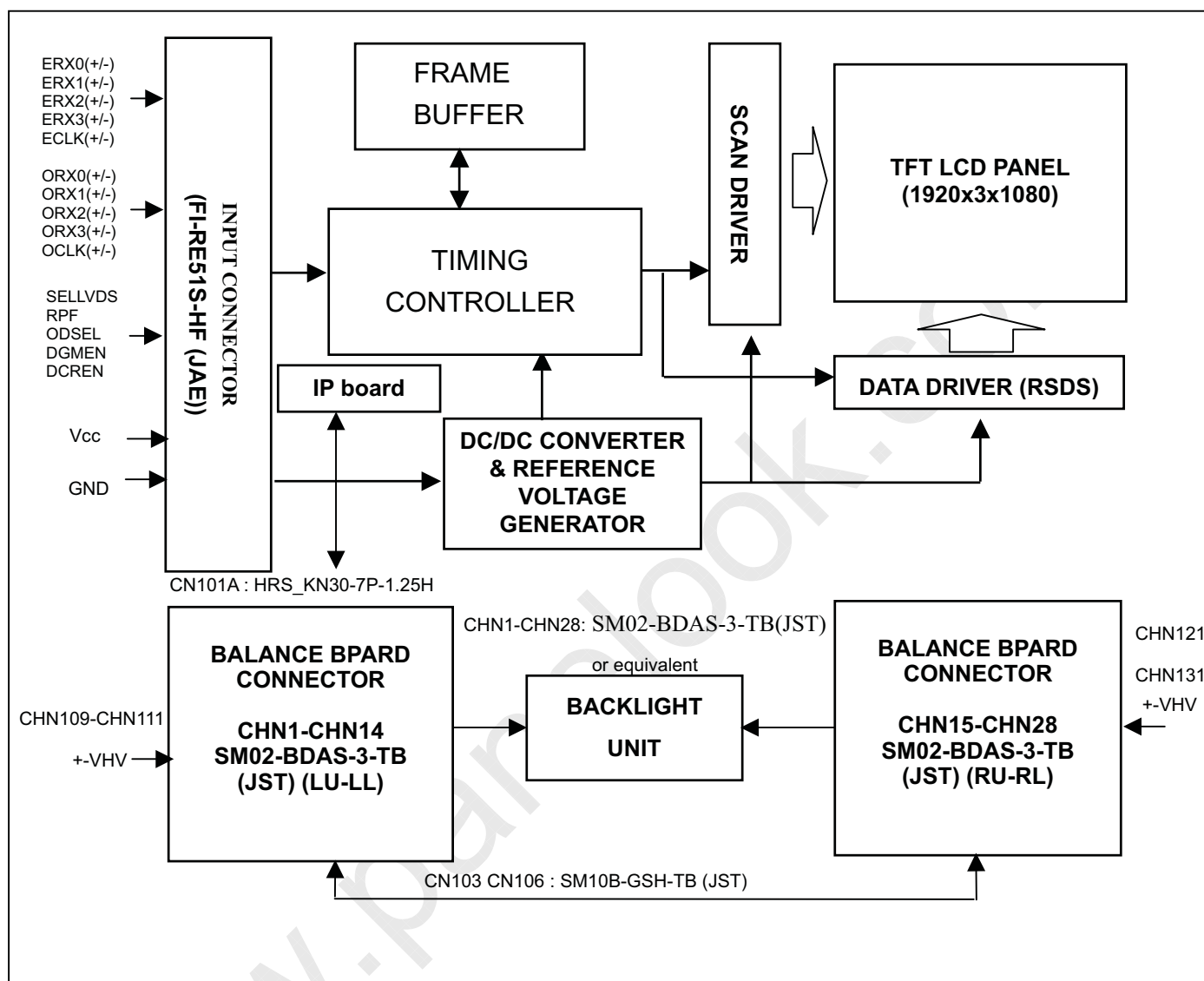
Note (2) The lamp starting voltage V_s should be applied to the lamp for more than 1 second after startup. Otherwise the lamp may not be turned on.





4. BLOCK DIAGRAM OF INTERFACE

4.1 TFT LCD MODULE



5. INPUT TERMINAL PIN ASSIGNMENT

5.1 TFT LCD Module Input

Pin	Name	Description	Note
1	VCC	+12V power supply	
2	VCC	+12V power supply	
3	VCC	+12V power supply	
4	VCC	+12V power supply	
5	VCC	+12V power supply	
6	GND	Ground	
7	GND	Ground	
8	GND	Ground	
9	GND	Ground	
10	ORX0-	Odd pixel Negative LVDS differential data input. Channel 0	
11	ORX0+	Odd pixel Positive LVDS differential data input. Channel 0	
12	ORX1-	Odd pixel Negative LVDS differential data input. Channel 1	
13	ORX1+	Odd pixel Positive LVDS differential data input. Channel 1	
14	ORX2-	Odd pixel Negative LVDS differential data input. Channel 2	
15	ORX2+	Odd pixel Positive LVDS differential data input. Channel 2	
16	GND	Ground	
17	OCLK-	Odd pixel Negative LVDS differential clock input.	
18	OCLK+	Odd pixel Positive LVDS differential clock input.	
19	GND	Ground	
20	ORX3-	Odd pixel Negative LVDS differential data input. Channel 3	
21	ORX3+	Odd pixel Positive LVDS differential data input. Channel 3	
22	N.C.	No Connection	(1)
23	N.C.	No Connection	
24	GND	Ground	
25	ERX0-	Even pixel, Negative LVDS differential data input. Channel 0	
26	ERX0+	Even pixel, Positive LVDS differential data input. Channel 0	
27	ERX1-	Even pixel, Negative LVDS differential data input. Channel 1	
28	ERX1+	Even pixel, Positive LVDS differential data input. Channel 1	
29	ERX2-	Even pixel, Negative LVDS differential data input. Channel 2	
30	ERX2+	Even pixel, Positive LVDS differential data input. Channel 2	
31	GND	Ground	
32	ECLK-	Even pixel, Negative LVDS differential clock input	
33	ECLK+	Even pixel, Positive LVDS differential clock input.	
34	GND	Ground	
35	ERX3-	Even pixel, Negative LVDS differential data input. Channel 3	
36	ERX3+	Even pixel, Positive LVDS differential data input. Channel 3	
37	N.C.	No Connection	(1)
38	N.C.	No Connection	
39	GND	Ground	
40	ODSEL	Overdrive Lookup Table Selection	(4)
41	DCREN	Dynamic Contrast Ratio Enable	(5)
42	N.C.	No Connection	(1)
43	RPF	Display Rotation	(3)
44	N.C.	No Connection	(1)
45	SELLVDS	LVDS Data Format Selection	(2)
46	N.C.	No Connection	(1)
47	N.C.	No Connection	
48	N.C.	No Connection	



49	N.C.	No Connection	(1)
50	N.C.	No Connection	
51	N.C.	No Connection	

Note (1) Reserved for internal use. Please leave it open.

Note (2) Low : JEIDA LVDS Format (default), High : VESA Format.

Note (3) Low : normal display (default), High : display with 180 degree rotation

Note (4) Overdrive lookup table selection. The overdrive lookup table should be selected in accordance with the frame rate to optimize image quality.

ODSEL	Note
L	Lookup table was optimized for 60 Hz frame rate.
H	Lookup table was optimized for 50 Hz frame rate.

Note (5) Low : function disable (default), High : Dynamic Contrast Ratio function enable.

Note (6) Low =Open or Connect to GND, High = Connect to +3.3V

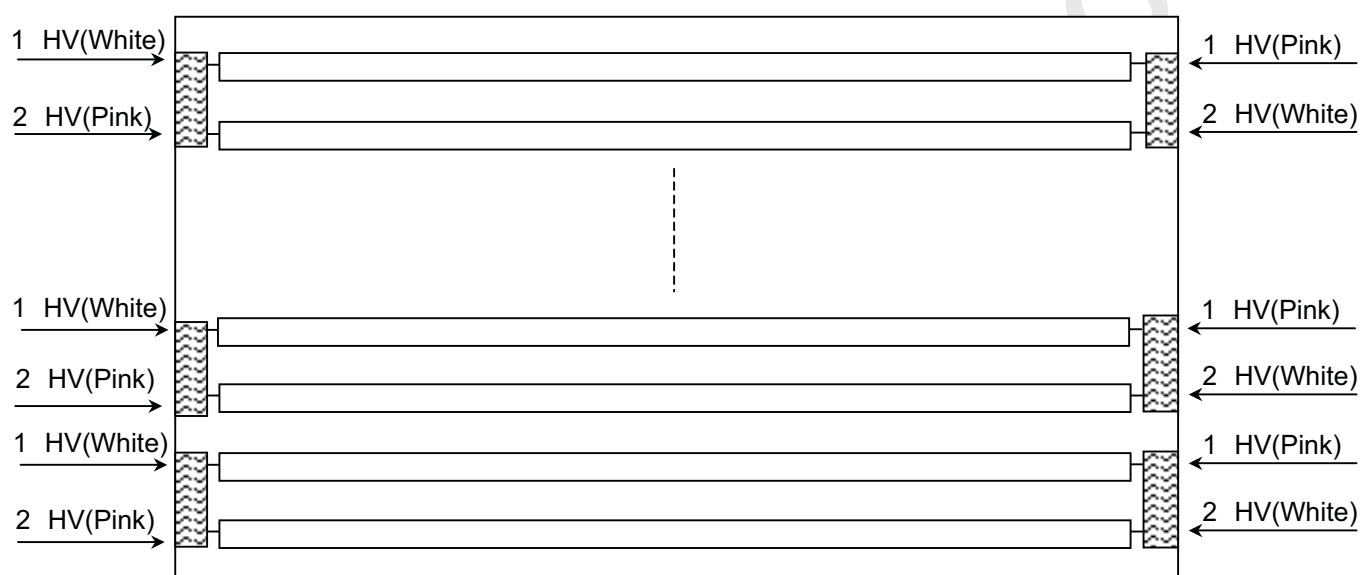
5.2 BACKLIGHT UNIT

The pin configuration for the housing and the leader wire is shown in the table below.

CN12-CN39: CP042CL000 (Cvilux).

Pin	Name	Description	Wire Color
1	HV	High Voltage	Pink
2	HV	High Voltage	White

Note (1) The backlight interface housing for high voltage side is a model CP042CL000, manufactured by Cvilux. The mating header on inverter part number is CP042CP1MB0



5.3 INVERTER UNIT

CHN109 , CHN111 , CHN121 , CHN131 : SM02B-BDAS-3-TB (D)(LF)(JST)

CHN1-28 : SM02B-BDAS-3-TB (D)(LF)(JST)

Connector	Pin	Symbol	Description	I/O
CHN109	1	HV-	High Voltage	Input
CHN111	2	HV+	High Voltage	
CHN121	1	HV-	High Voltage	
CHN131	2	HV+	High Voltage	
CHN1-28	1	HV+	High Voltage	Output
	2	HV-	High Voltage	

CN101A : HRS_KN30-7P-1.25H

Pin №	Symbol	Feature
1	VCC	Supply voltage of balance board
2	PROTECTION	PROTECTION
3	GND	GND
4	GND	
5	NC	NC
6	I_SNS	Lamp Detection
7	I_SNS	

CN103 , CN106 : SM10B-GSH-TB (JST)

CN126 CN225 Pin №	Symbol	Description
1	Control Signal	Board to Board
2		Board to Board
3		Board to Board
4		Board to Board
5		Board to Board
6		Board to Board
7		Board to Board
8		Board to Board
9		Board to Board
10		Board to Board

CHN110 , CHN112 , CHN122 , CHN132 : SM02B-BDAS-3-TB (D)(LF)(JST)

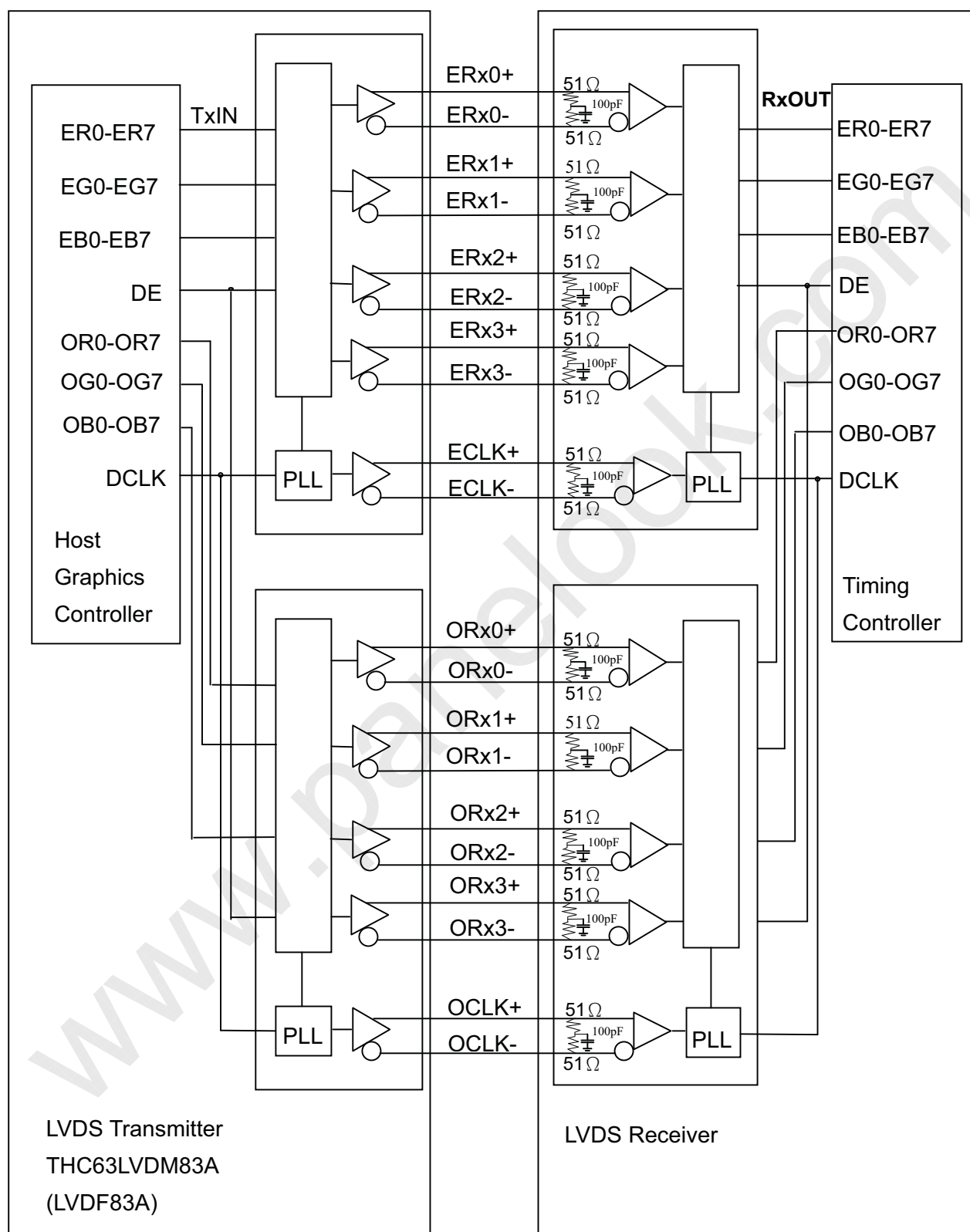
Connector	Pin	Symbol	Description
CHN109	1	HV-	Board to Board
CHN111	2	HV+	Board to Board
CHN121	1	HV-	Board to Board
CHN131	2	HV+	Board to Board



CN102 , CN104 , CN105 : SM07B-GHS-TBT(JST)

Pin No	Symbol	Feature
1	Control Signal	Board to Board
2		Board to Board
3		Board to Board
4		Board to Board
5		Board to Board
6		Board to Board
7		Board to Board

5.4 BLOCK DIAGRAM OF INTERFACE



ER0~ER7 : Even pixel R data

EG0~EG7 : Even pixel G data

EB0~EB7 : Even pixel B data

OR0~OR7 : Odd pixel R data

OG0~OG7 : Odd pixel G data

OB0~OB7 : Odd pixel B data

DE : Data enable signal

DCLK : Data clock signal

- Notes:
- (1) The system must have the transmitter to drive the module.
 - (2) LVDS cable impedance shall be 50 ohms per signal line or about 100 ohms per twist-pair line when it is used differentially.
 - (3) Two pixel data send into the module for every clock cycle. The first pixel of the frame is odd pixel and the second pixel is even pixel.

**5.5 LVDS INTERFACE**

	SIGNAL		TRANSMITTER THC63LVDM83A		INTERFACE CONNECTOR		RECEIVER THC63LVDF84A		TFT CONTROL INPUT	
	LVDS_SEL =H	LVDS_SEL = L or OPEN	PIN	INPUT	Host	TFT-LCD	PIN	OUTPUT	LVDS_SEL =H	LVDS_SEL = L or OPEN
24bit	R0	R2	51	TxIN0	TA OUT0+	Rx 0+	27	Rx OUT0	R0	R2
	R1	R3	52	TxIN1			29	Rx OUT1	R1	R3
	R2	R4	54	TxIN2			30	Rx OUT2	R2	R4
	R3	R5	55	TxIN3			32	Rx OUT3	R3	R5
	R4	R6	56	TxIN4	TA OUT0-	Rx 0-	33	Rx OUT4	R4	R6
	R5	R7	3	TxIN6			35	Rx OUT6	R5	R7
	G0	G2	4	TxIN7			37	Rx OUT7	G0	G2
	G1	G3	6	TxIN8			38	Rx OUT8	G1	G3
	G2	G4	7	TxIN9	TA OUT1+	Rx 1+	39	Rx OUT9	G2	G4
	G3	G5	11	TxIN12			43	Rx OUT12	G3	G5
	G4	G6	12	TxIN13			45	Rx OUT13	G4	G6
	G5	G7	14	TxIN14			46	Rx OUT14	G5	G7
	B0	B2	15	TxIN15	TA OUT1-	Rx 1-	47	Rx OUT15	B0	B2
	B1	B3	19	TxIN18			51	Rx OUT18	B1	B3
	B2	B4	20	TxIN19			53	Rx OUT19	B2	B4
	B3	B5	22	TxIN20			54	Rx OUT20	B3	B5
	B4	B6	23	TxIN21	TA OUT2+	Rx 2+	55	Rx OUT21	B4	B6
	B5	B7	24	TxIN22			1	Rx OUT22	B5	B7
	DE	DE	30	TxIN26			6	Rx OUT26	DE	DE
	R6	R0	50	TxIN27	TA OUT2-	Rx 2-	7	Rx OUT27	R6	R0
	R7	R1	2	TxIN5			34	Rx OUT5	R7	R1
	G6	G0	8	TxIN10			41	Rx OUT10	G6	G0
	G7	G1	10	TxIN11			42	Rx OUT11	G7	G1
	B6	B0	16	TxIN16	TA OUT3+	Rx 3+	49	Rx OUT16	B6	B0
	B7	B1	18	TxIN17			50	Rx OUT17	B7	B1
	RSVD 1	RSVD 1	25	TxIN23			2	Rx OUT23	NC	NC
	RSVD 2	RSVD 2	27	TxIN24	TA OUT3-	Rx 3-	3	Rx OUT24	NC	NC
	RSVD 3	RSVD 3	28	TxIN25			5	Rx OUT25	NC	NC
	DCLK		31	TxCLK IN	TxCLK OUT+	RxCLK IN+	26	RxCLK OUT	DCLK	
					TxCLK OUT-	RxCLK IN-				

R0~R7: Pixel R Data (7; MSB, 0; LSB)

G0~G7: Pixel G Data (7; MSB, 0; LSB)

B0~B7: Pixel B Data (7; MSB, 0; LSB)

DE : Data enable signal

DCLK : Data clock signal

Notes: (1) RSVD (reserved) pins on the transmitter shall be "H" or "L".

5.6 COLOR DATA INPUT ASSIGNMENT

The brightness of each primary color (red, green and blue) is based on the 8-bit gray scale data input for the color. The higher the binary input, the brighter the color. The table below provides the assignment of the color versus data input.

Color		Data Signal																							
		Red								Green								Blue							
		R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale Of Red	Red (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (1)	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (2)	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
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	Red (253)	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (254)	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Gray Scale Of Green	Green (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	Green (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Green (253)	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0
	Green (254)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
	Green (255)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
Gray Scale Of Blue	Blue (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Blue (253)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1
	Blue (254)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0
	Blue (255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Note (1) 0: Low Level Voltage, 1: High Level Voltage

6. INTERFACE TIMING

6.1 INPUT SIGNAL TIMING SPECIFICATIONS

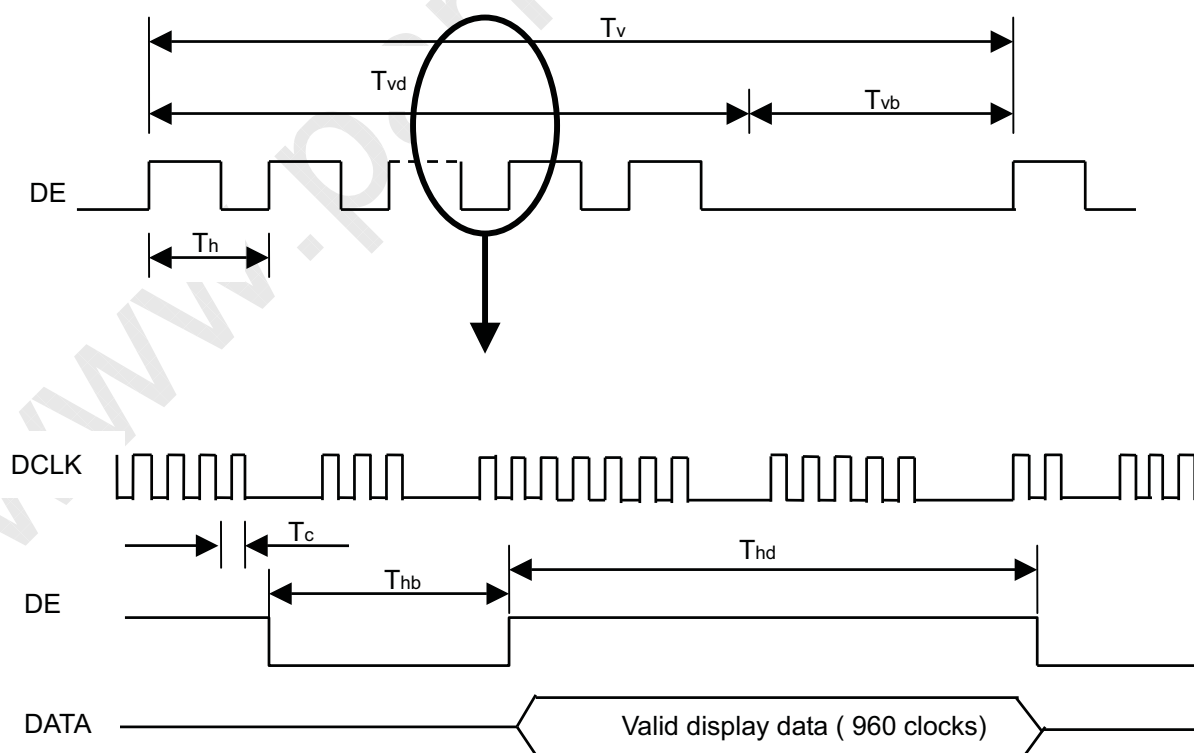
The input signal timing specifications are shown as the following table and timing diagram.

Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
LVDS Receiver Clock	Frequency	1/Tc	60	74	80	MHz	-
	Input cycle to cycle jitter	Trcl	-	-	200	ps	-
LVDS Receiver Data	Setup Time	Tlvsu	600	-	-	ps	-
	Hold Time	Tlvhd	600	-	-	ps	-
Vertical Active Display Term	Frame Rate	Fr5	47	50	53	Hz	(1)
		Fr6	57	60	63	Hz	(1)
	Total	Tv	1115	1125	1135	Th	Tv=Tvd+Tvb
	Display	Tvd	1080	1080	1080	Th	-
	Blank	Tvb	35	45	55	Th	-
Horizontal Active Display Term	Total	Th	2100	2200	2300	Tc	Th=Thd+Thb
	Display	Thd	1920	1920	1920	Tc	-
	Blank	Thb	180	280	380	Tc	-

Note (1) (ODSEL) = (H) , (L). Please refer to 5.1 for detail information.

Note (2) Since the module is operated in DE only mode, Hsync and Vsync input signals should be set to low logic level. Otherwise, this module would operate abnormally.

INPUT SIGNAL TIMING DIAGRAM





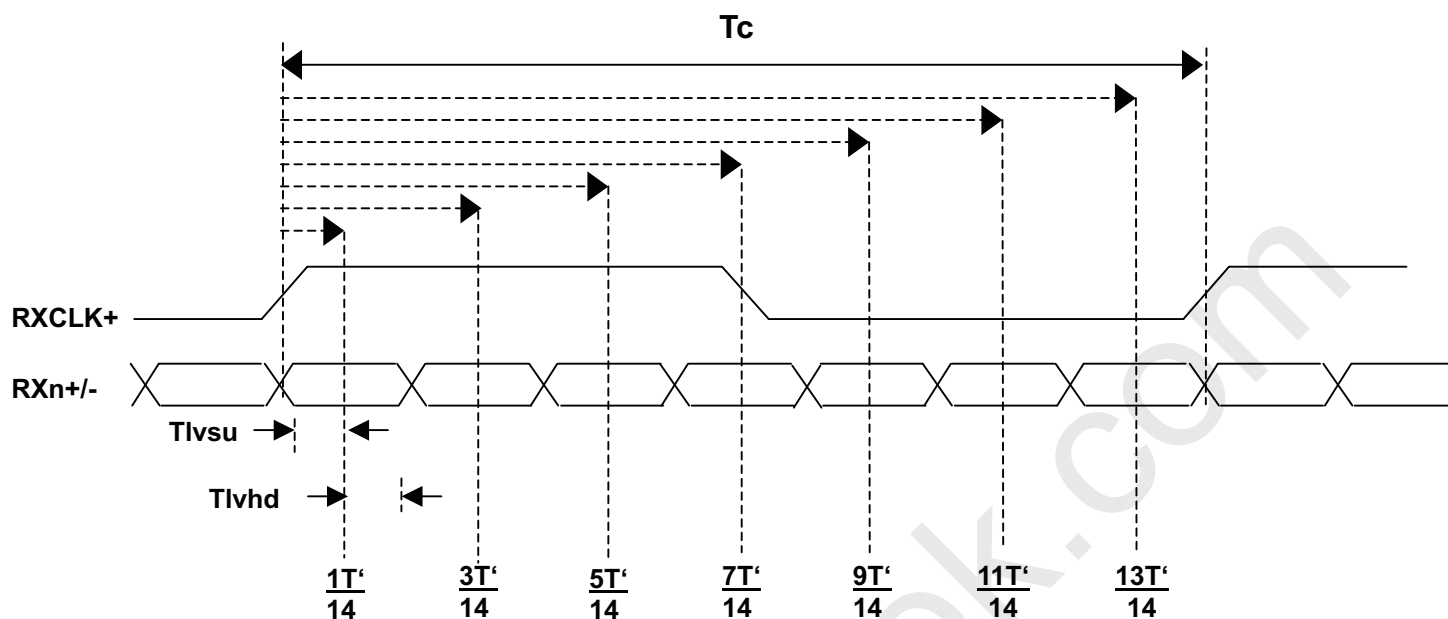
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Model No.:V520H1-L05

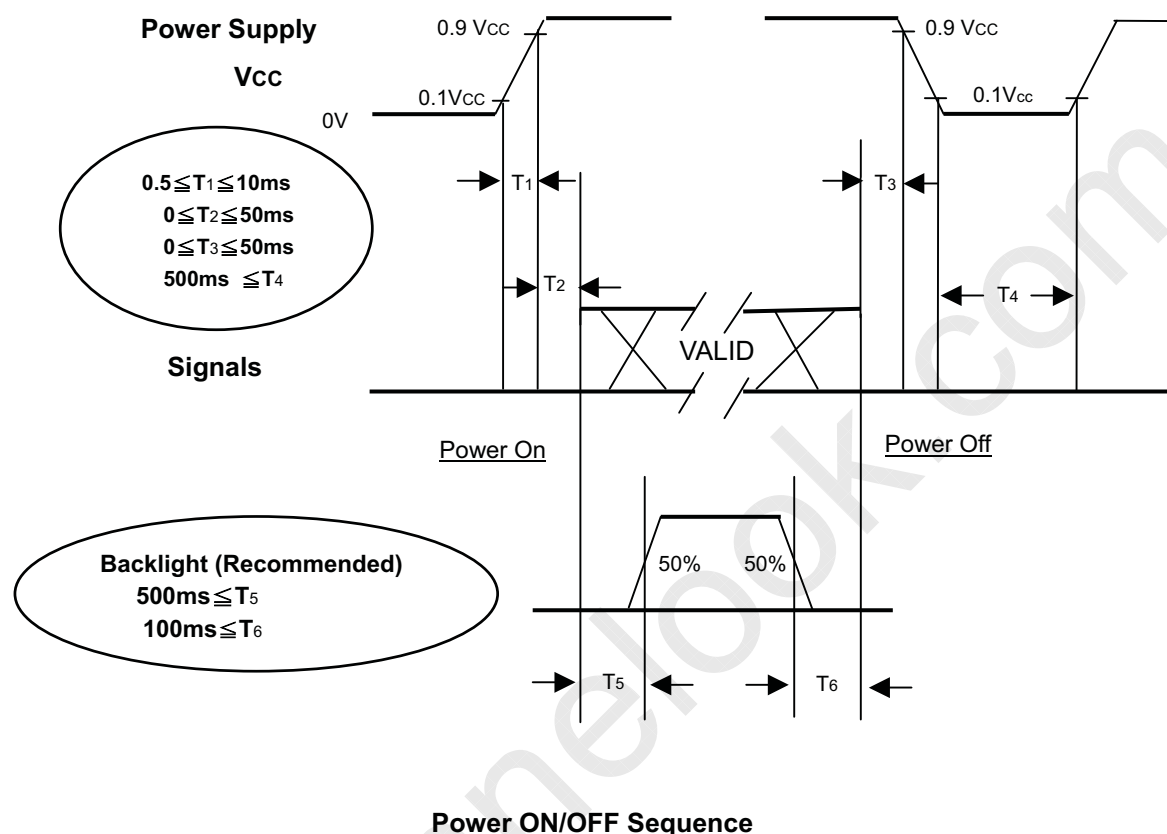
Preliminary

LVDS INPUT INTERFACE TIMING DIAGRAM



6.2 POWER ON/OFF SEQUENCE

To prevent a latch-up or DC operation of LCD module, the power on/off sequence should follow the diagram below.



Note.

- (1) The supply voltage of the external system for the module input should follow the definition of Vcc.
- (2) Apply the lamp voltage within the LCD operation range. When the backlight turns on before the LCD operation or the LCD turns off before the backlight turns off, the display may momentarily become abnormal screen.
- (3) In case of VCC is in off level, please keep the level of input signals on the low or high impedance.
- (4) T4 should be measured after the module has been fully discharged between power off and on period.
- (5) Interface signal shall not be kept at high impedance when the power is on.

7. OPTICAL CHARACTERISTICS

7.1 TEST CONDITIONS

Item	Symbol	Value	Unit
Ambient Temperature	Ta	25±2	°C
Ambient Humidity	Ha	50±10	%RH
Supply Voltage	V _{CC}	12/18	V
Input Signal	According to typical value in "3. ELECTRICAL CHARACTERISTICS"		
Lamp Current	I _L	6.0±0.5	mA
Oscillating Frequency (Inverter)	F _W	50±3	KHz
Vertical Frame Rate	Fr	60	Hz

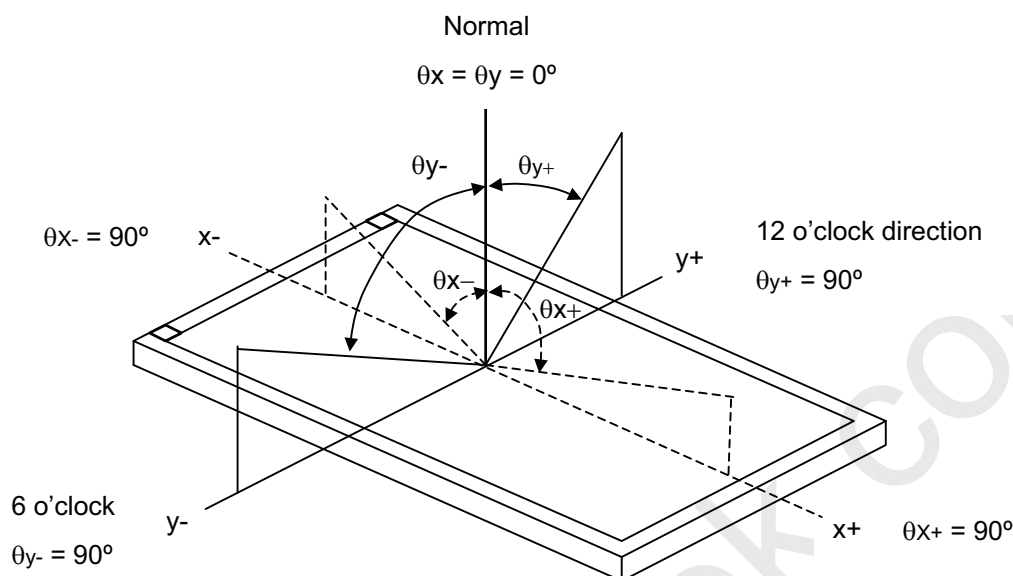
7.2 OPTICAL SPECIFICATIONS

The relative measurement methods of optical characteristics are shown in 7.2. The following items should be measured under the test conditions described in 7.1 and stable environment shown in Note (6).

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Contrast Ratio		CR	$\theta_x=0^\circ, \theta_y=0^\circ$ Viewing Angle at Normal Direction		1500		-	Note (2)
		Dynamic CR			6000			
Response Time		Gray to gray			6.5		ms	Note (3)
Center Luminance of White		L _c			550		cd/m ²	Note (4)
White Variation		δW				1.3	-	Note (7)
Cross Talk		CT				4	%	Note (5)
Color Chromaticity	Red	R _x		Typ. -0.03	0.658	Typ. +0.03	-	Note (6)
		R _y			0.327		-	
	Green	G _x			0.189		-	
		G _y			0.670		-	
	Blue	B _x			0.152		-	
		B _y			0.059		-	
	White	W _x			0.280		-	
		W _y			0.290		-	
	Color Gamut	C.G			92		%	NTSC
Viewing Angle	Horizontal	θ_{x+}	CR≥20	80	88		Deg.	Note (1)
		θ_{x-}		80	88			
	Vertical	θ_{y+}		80	88			
		θ_{y-}		80	88			

Note (1) Definition of Viewing Angle (θ_x , θ_y):

Viewing angles are measured by Eldim EZ-Contrast 160R



Note (2) Definition of Contrast Ratio (CR):

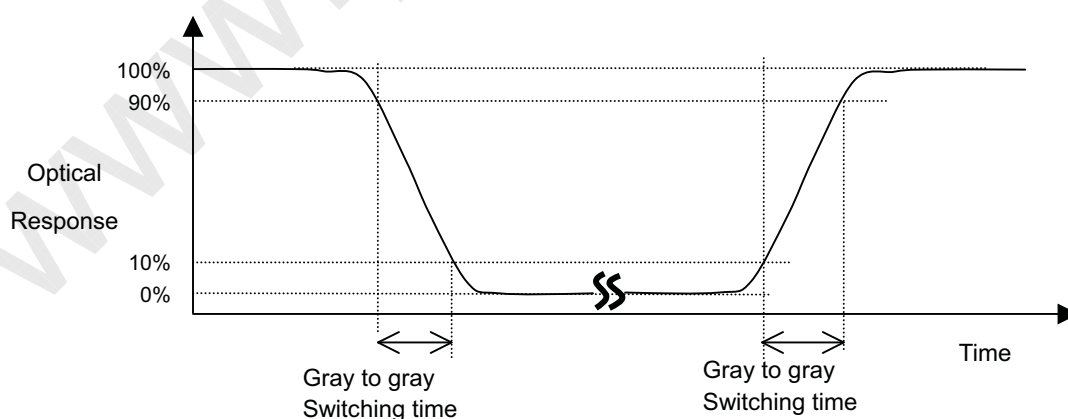
The contrast ratio can be calculated by the following expression.

$$\text{Contrast Ratio (CR)} = \frac{\text{Surface Luminance with all white pixels}}{\text{Surface Luminance with all black pixels}}$$

CR = CR (5), where CR (X) is corresponding to the Contrast Ratio of the point X at the figure in Note (7).

The measured value will be "Dynamic CR" only when the function of dynamic contrast ratio is enabled.

Note (3) Definition of Gray-to-Gray Switching Time:



The driving signal means the signal of gray level 0, 63, 127, 191, and 255.

Gray to gray average time means the average switching time of gray level 0, 63, 127, 191, 255 to each other.

Note (4) Definition of Luminance of White (L_C , L_{AVE}):

Measure the luminance of gray level 255 at center point and 5 points

$L_C = L(5)$, where $L(X)$ is corresponding to the luminance of the point X at the figure in Note (7).

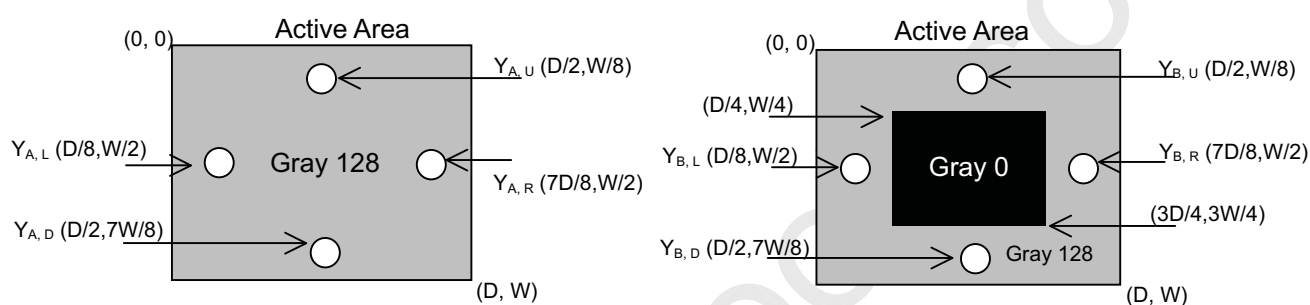
Note (5) Definition of Cross Talk (CT):

$$CT = |Y_B - Y_A| / Y_A \times 100 (\%)$$

Where:

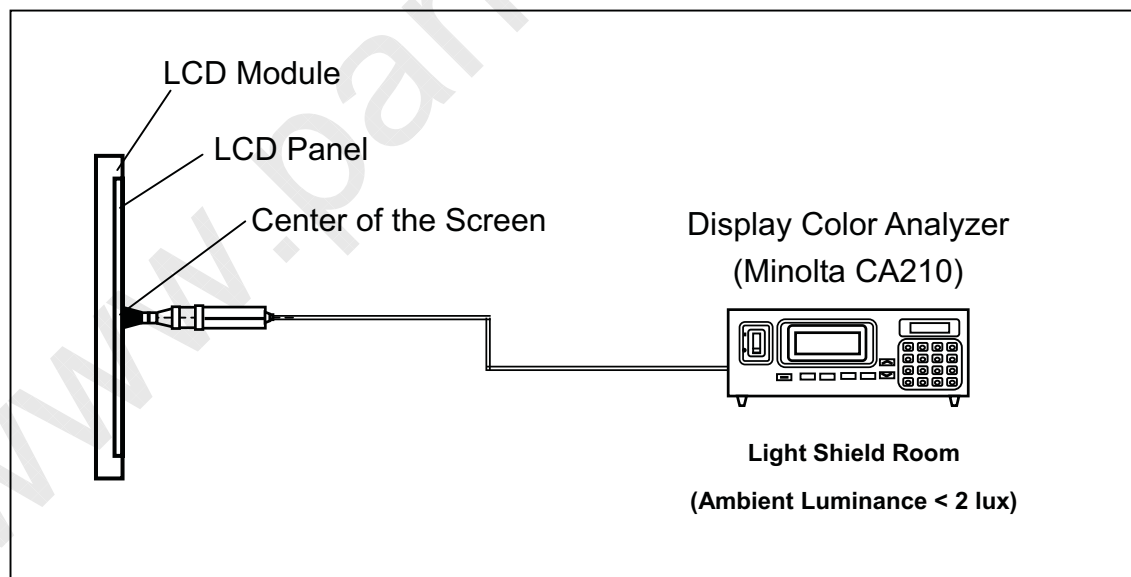
Y_A = Luminance of measured location without gray level 0 pattern (cd/m^2)

Y_B = Luminance of measured location with gray level 0 pattern (cd/m^2)



Note (6) Measurement Setup:

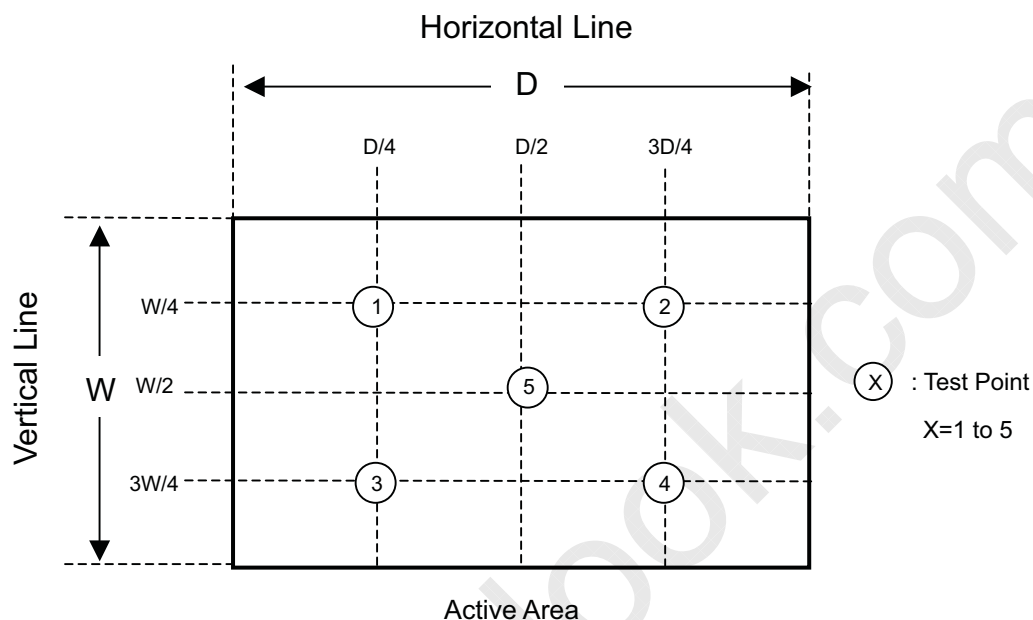
The LCD module should be stabilized at given temperature for 1 hour to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting backlight for 1 hour in a windless room.



Note (7) Definition of White Variation (δW):

Measure the luminance of gray level 255 at 5 points

$$\delta W = \text{Maximum [L (1), L (2), L (3), L (4), L (5)]} / \text{Minimum [L (1), L (2), L (3), L (4), L (5)]}$$



8. PRECAUTIONS

8.1 ASSEMBLY AND HANDLING PRECAUTIONS

- (1) Do not apply rough force such as bending or twisting to the module during assembly.
- (2) It is recommended to assemble or to install a module into the user's system in clean working areas. The dust and oil may cause electrical short or worsen the polarizer.
- (3) Do not apply pressure or impulse to the module to prevent the damage of LCD panel and Backlight.
- (4) Always follow the correct power-on sequence when the LCD module is turned on. This can prevent the damage and latch-up of the CMOS LSI chips.
- (5) Do not plug in or pull out the I/F connector while the module is in operation.
- (6) Do not disassemble the module.
- (7) Use a soft dry cloth without chemicals for cleaning, because the surface of polarizer is very soft and easily scratched.
- (8) Moisture can easily penetrate into LCD module and may cause the damage during operation.
- (9) High temperature or humidity may deteriorate the performance of LCD module. Please store LCD modules in the specified storage conditions.
- (10) When ambient temperature is lower than 10°C, the display quality might be reduced. For example, the response time will become slow, and the starting voltage of CCFL will be higher than that of room temperature.

8.2 SAFETY PRECAUTIONS

- (1) The startup voltage of a Backlight is approximately 1000 Volts. It may cause an electrical shock while assembling with the inverter. Do not disassemble the module or insert anything into the Backlight unit.
- (2) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, skin or clothes, it has to be washed away thoroughly with soap.
- (3) After the module's end of life, it is not harmful in case of normal operation and storage.

8.3 SAFETY STANDARDS

The LCD module should be certified with safety regulations as follows:

- (1) UL60950-1 or updated standard.
- (2) IEC60950-1 or updated standard.
- (3) UL60065 or updated standard.
- (4) IEC60065 or updated standard.

9. PACKAGING

9.1 PACKING SPECIFICATIONS

- (1) 2 LCD TV modules / 1 Box
- (2) Box dimensions : 1334(L) X 284 (W) X 856 (H)
- (3) Weight : approximately 47.5Kg (2 modules per box)

9.2 PACKING METHOD

Figures 9-1 and 9-2 are the packing method

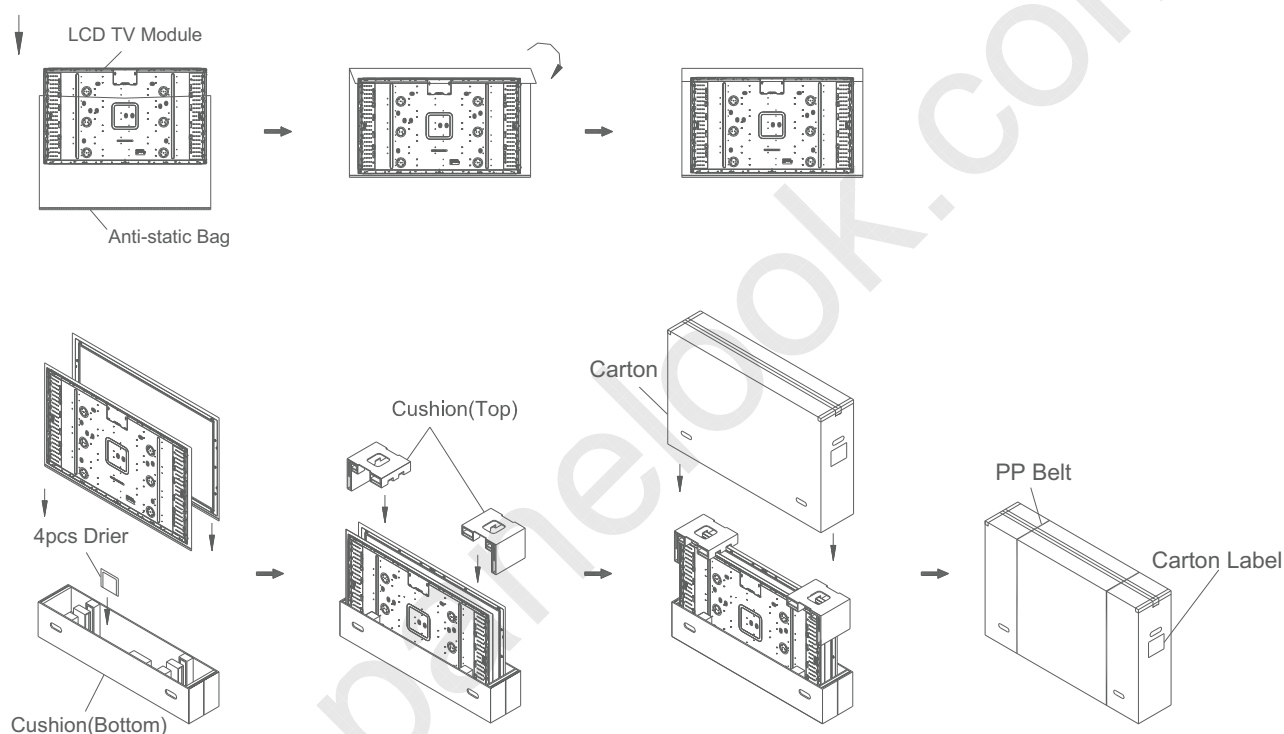
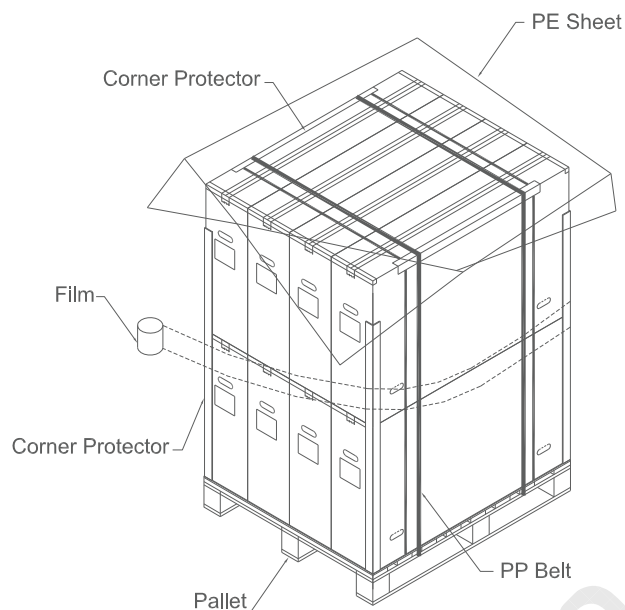


Figure. 9-1 packing method

Sea Transportation

Corner Protector:L1780*50mm*50mm
Corner Protector:L1130*50mm*50mm
Pallet:L1150*W1345*H140mm
Pallet Stack:L1150*W1345*H1852mm
Gross: 400 kg



Air Transportation

Corner Protector:L800*50mm*50mm
Corner Protector:L1130*50mm*50mm
Pallet:L1150*W1345*H140mm
Pallet Stack:L1150*W1345*H996mm
Gross: 210 kg

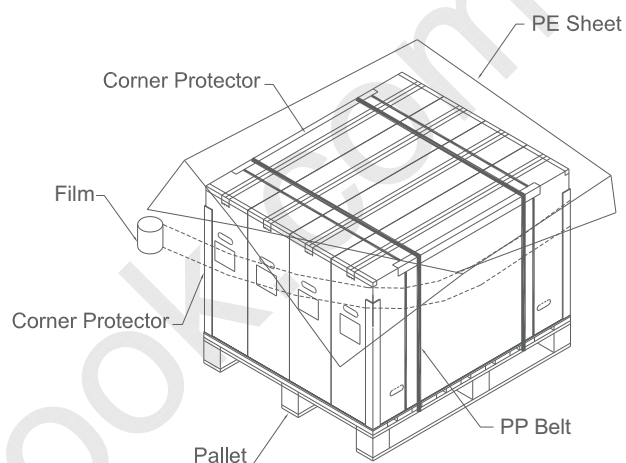


Figure. 9-2 Packing method



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Issue Date: Apr.10.2007

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